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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/583,797	06/21/2006	Erik Petrus Antonius Maria Bakkers	NL03 1483 US1	6881

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EXAMINER	
WOLDEGEORGIS, ERMIAS T	
ART UNIT	PAPER NUMBER
2893	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/583,797	BAKKERS ET AL.	
	Examiner	Art Unit	
	ERMIAS WOLDEGEORGIS	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2006* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/21/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. *Priority*

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

2. *Information Disclosure Statement*

The information disclosure statement (IDS) filed on 1/30/2008 has been acknowledged and a signed copy of the PTO-1449 are attached herein.

3. *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claim 15 is rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al. **(US Pat No. 6773616 B1, hereinafter "Chen")**.

In regards to claim 15, Chen discloses (Figures 5a and 5b) a method of growing a second material in epitaxial relationship with a first material **(Growth of ErSi2 on Si, column 7 lines 50-55)**, the second material **(ErSi2)** and the first material **(Si)** having a mutual lattice mismatch **(6.3%, column 7 lines 20-26)**, the method comprising the steps of: providing a substrate **(Si substrates, column 7 lines 60-61)** of the first

material, forming a nanostructure **(ErSi2 nanowires, column 8 lines 30)** of the second material by a growth method **(column 8 lines 1-7 and 30-31)**, wherein the first material **(ErSi2)** comprising at least one element from a first group **(Er)** in the periodic table and the second material **(Si)** comprising at least one element from a second group **(Si)**, the second group **(Si)** being different from the first group **(Si)**, and wherein the nanostructure being supported by and in epitaxial relationship **(epitaxial overlayer … carefully chosen lattice mismatch… in this case erbium disilicide, column 7 lines 55-58)** with the substrate**(Si substrates, column 7 lines 7 lines 60-61)**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 4-5, 6-11, and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Graham et el. WO 2004/040668 ("Graham") (see also **US PG-Pub 2005/0224888 A1)** in view of Chen.

In regards to claim 1, Graham discloses (Figure 4) an electric device comprising: a substrate **(101)** having a main surface of a first material **(glass substrate, Par [0046] of US PG-Pub, a quartz substrate, …, a silicon wafer, Par [0031] of US PG-Pub)**, and a nanostructure **(301)** of a second material **(carbon nanotube, Par [0048] of US PG-**

Pub), wherein the first and second materials having a mutual lattice mismatch **(inherently different materials has lattice mismatch)**, and wherein the nanostructure **(301)** being supported by **(102)** the substrate **(101)**.

Graham fails to disclose the nanostructure is in epitaxial relationship with the substrate.

Chen while disclosing method of formatting on dimensional crystalline nanowires **(abstract)** teaches growing epitaxial layer on substrate to better control the lattice mismatch between the two materials **(column 3 lines 37-62).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to epitaxially grow the second material on the substrate with carefully selected material because in doing so the lattice mismatch would be controlled and reduced to the acceptable level below 4% so that the growth won't be limited in all directions as taught by Chen in **column 20-35.**

In regards to claim 2, Graham discloses (Figure 4) the nanostructure **(301)** is in electrical contact **(through the Ni layer 102, see Figure 4)** with the substrate **(101)**.

In regards to claim 3, Graham as modified by Chen (Figure 4, Graham) discloses all limitations of claims 1 and 2 above except that the resistance between the nanostructure and the substrate is below 10^{-5} Ohm cm2.

Chen teaches the conductivity to be $2.9X10^4$ $(\Omega.cm)^{-1}$ **(column 7 lines 58-59)** and the average lengths of the nanowires is between 150 to 450nm **(column 7 lines 30-33).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to keep the contact resistance low because this would help improve the device performance.

In regards to claim 4, Graham discloses the nanostructure **(301)** is a nanotube **(carbon nanotube, Par [0038] of US PG-Pub)**.

In regards to claim 5, Graham discloses all limitations of claim 1 above except a lattice mismatch between the substrate and the nanostructure(s) is smaller than 10%.

Chen discloses a lattice mismatch between the substrate **(Si substrates, column 7 lines 60-61)** and the nanostructure(s) **(ErSi2 nanowires, column 8 lines 30)** is smaller than 10% **(6.3%, column 7 lines 20-26)**.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Graham by Chen because as the lattice mismatch between the lattice mismatch increases above 10% it makes it difficult to grow atomically flat two-dimensional epitaxial overlayer as the strain energy in the deposited

film can be relaxed by the creation of islands of the epitaxial material. And, this will limit the lateral growth in all directions on the substrate surface as taught by Chen in **column 3 lines 20-35.**

In regards to claim 6, Graham discloses (Figure 4) the nanostructure **(301)** is a substantially single-crystal nanostructure **(carbon nanotube, Par [0038])**.

In regards to claim 7, Graham discloses (Figure 4) a plurality of nanostructures **(301)** are arranged in an array **(Field effect transistors 404, 403, ...)**.

In regards to claim 8, Graham discloses (Figure 4) the electric device **(400)** is a gate-around transistor **(Par [0042] of US PG-Pub).**

In regards to claim 9, Graham discloses (Figure 4) a first dielectric **(104)** and wherein the first dielectric **(104)** is in contact with at least a section of the nanostructure **(301)**.

In regards to claim 10, Graham discloses (Figure 4) a first conductive material **(201)** and wherein the first conductive material **(201)** is electrically insulated from the substrate **(101)** by the first dielectric **(104)**.

In regards to claim 11, Graham discloses (Figure 4) a second dielectric **(303)** and wherein the second dielectric **(303)** is electrically insulating the first conductive material **(201)** from the nanostructure **(301)**.

In regards to claim 13, Graham discloses (Figure 4) a second conductive material **(402)** and wherein the second conductive material **(402)** is in contact with at least one nanostructure **(301)**.

In regards to claim 14, Graham discloses (Figure 4) at least a third dielectric **(203)**, the at least third dielectric **(203)** insulating the second conductive material **(402)** from the first conductive material **(201)**.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Graham in view of Chen as applied to claims 1 and 8-11 above, and further in view of Roesner et al. **(US Pat No. 6740910 B2, hereinafter "Roesner")**.

In regards to claim 12, Graham discloses (Figure 4) the first dielectric **(104)** and the second dielectric **(303).**

Graham fails to teach that the first dielectric is thicker than the second dielectric.

Roesner while disclosing a field effect transistor with a nanelement forming channel region **(abstract)** teaches the first dielectric material **103** has a layer thickness of approximately 20 nm **(column 5 lines 19-21)** and the through holes **106** have a diameter of approximately 1nm to 10nm **(column 5 lines 48-51).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the first dielectric layer thicker than the second dielectric layer because this would help safely insulate the gate electrode from the source layer and help enhance the performance of the field effect transistor as the dielectric layer gets thinner and thinner in the gate area for the high-K material such as dialuminum trioxide.

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Chen et al. **(PG Pub No. US 2004/0137214 A1, hereinafter "Chen'214")**.

In regards to claim 16, Chen discloses (Figure 4) the nanostructure **(ErSi2 nanowires, column 8 lines 30).**

Chen fails to teach that the nanostructure is grown according to the vapour-liquid-solid growth method.

Chen'214 while disclosing a material with a surface nanometer functional structure teaches growing nanostructures using vapor-liquid-solid method **(abstract).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use VLS method to grow nanostructures because one would find it easier to control the diameter of the nanowires by the catalyst granular size as taught by Chen'214 in **Par [0007].**

8. ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERMIAS WOLDEGEORGIS whose telephone number is (571)270-5350. The examiner can normally be reached on Monday through Friday 8:30 AM to 6:00 PM E.S.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Daveinne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ERMIAS WOLDEGEORGIS/
Examiner, Art Unit 2893

/A. Sefer/
Primary Examiner
Art Unit 2893